Amendments to the Claims

LISTING OF CLAIMS

Claims 1-50 (canceled)

51. (currently amended) A method for fabricating a semiconductor component comprising:

providing a base die comprising a substrate having a back side;

thinning the base die;

forming a plurality of conductive vias in the substrate;

providing a secondary die comprising a circuit side and a plurality of contacts;

bonding the secondary die to the back side and the contacts to the conductive vias; ~~and~~

thinning the secondary die; and

forming a plurality of terminal contacts on the base die in electrical communication with the conductive vias.

52. (currently amended) The method of claim 51 further comprising forming an encapsulant on the back side at least partially encapsulating the secondary die.
~~prior to the bonding step thinning the base die, and following the bonding step thinning the secondary die.~~

53. (currently amended) ~~The method of claim 51 further comprising~~

A method for fabricating a semiconductor component comprising:

providing a base die comprising a substrate having a back side;

forming a plurality of conductive vias in the substrate;

providing a secondary die comprising a circuit side and a plurality of contacts;

bonding the secondary die to the back side and the contacts to the conductive vias;

forming a plurality of terminal contacts on the base die in electrical communication with the conductive vias; and

forming a polymer layer on the base die proximate to the terminal contacts configured to protect and rigidify the component.

54. (currently amended) ~~The method of claim 51 wherein~~

A method for fabricating a semiconductor component comprising:

providing a base die comprising a substrate having a back side;

forming a plurality of conductive vias in the substrate, the forming the conductive vias step comprising ~~comprises~~ laser machining openings from the back side into the substrate, forming insulating layers in the openings and depositing a conductive material in the openings;

providing a secondary die comprising a circuit side and a plurality of contacts;

bonding the secondary die to the back side and the contacts to the conductive vias;

forming a plurality of terminal contacts on the base die in electrical communication with the conductive vias.

55. (currently amended) ~~The method of claim 51 wherein~~

A method for fabricating a semiconductor component comprising:

providing a base die comprising a substrate having a back side;

forming a plurality of conductive vias in the substrate, the forming the conductive vias step comprising ~~comprises~~ forming openings in the substrate, depositing a metal in the openings and then squeegeeing a solder into the openings;

providing a secondary die comprising a circuit side and a plurality of contacts;

bonding the secondary die to the back side and the contacts to the conductive vias;

forming a plurality of terminal contacts on the base die in electrical communication with the conductive vias.

56. (previously presented) A method for fabricating a semiconductor component comprising:

providing a base die comprising a circuit side, a back side, a semiconductor substrate and a plurality of conductive vias in the substrate;

providing a secondary die comprising a plurality of contacts;

bonding the secondary die to the back side and the contacts to the conductive vias; and

forming a plurality of terminal contacts on the circuit side in electrical communication with the conductive vias.

57. (previously presented) The method of claim 56 further comprising forming an encapsulant on the back side at least partially encapsulating the secondary die.

58. (previously presented) The method of claim 56 wherein the base die is contained on a base wafer containing a plurality of base dice and the bonding step is performed by placing a plurality of secondary dice on the base dice.

59. (previously presented) The method of claim 56 wherein the base die is contained on a base wafer containing a plurality of base dice, the secondary die is contained on a secondary wafer containing a plurality of secondary dice and the bonding step is performed by bonding the base wafer to the secondary wafer.

60. (previously presented) The method of claim 56 further comprising forming a polymer layer on the circuit side configured as a stencil for forming the terminal contacts.

61. (previously presented) The method of claim 56 wherein the base die and the secondary die comprise thinned dice.

62. (previously presented) A method for fabricating a semiconductor component comprising:

providing base die on a base wafer;

forming a plurality of conductive vias on the base die;

providing a secondary die comprising a plurality of contacts;

bonding the secondary die to the base die with the contacts in electrical communication with the conductive vias;

thinning the secondary die while bonded to the base die on the wafer;

forming a plurality of terminal contacts on the base die in electrical communication with the conductive vias; and

singulating the base die with the secondary die bonded thereto from the wafer.

63. (previously presented) The method of claim 62 further comprising thinning the base die on the base wafer prior to the bonding step.

64. (currently amended) The method of claim 62 wherein the forming the conductive vias step comprises forming openings in the base die and at least partially filling the openings with a metal, a conductive polymer, or a nano particle conductive polymer.

65. (previously presented) The of claim 62 further comprising testing the secondary die and the base die prior to the bonding step.

66. (previously presented) The method of claim 62 further comprising following the singulating step mounting the base die to a module substrate.

67. (previously presented) The method of claim 62 wherein the secondary die is contained on a secondary wafer and the bonding step is performed by bonding the secondary wafer to the base wafer.

68. (previously presented) A method for fabricating a semiconductor component comprising:

providing a tested singulated secondary die comprising a plurality of bumped contacts;

providing a wafer comprising a base die comprising a substrate having a circuit side and a back side, a plurality of integrated circuits in the substrate, and a plurality of contacts on the substrate in electrical communication with the integrated circuits;

forming a polymer layer on the circuit side having openings aligned with the contacts;

forming a plurality of conductive vias in the back side extending through the substrate to the contacts;

bonding the secondary die to the back side with the bumped contacts in electrical communication with the conductive vias; and

forming terminal contacts in the openings using the polymer layer as a stencil.

69. (previously presented) The method of claim 68 wherein the forming the polymer layer step is performed using a laser imaging process.

70. (previously presented) The method of claim 68 wherein the laser imaging process comprises heat curing or UV curing the polymer layer.

71. (previously presented) The method of claim 68 wherein the forming the polymer layer step comprises depositing and curing a polymer material.

72. (previously presented) The method of claim 68 wherein the forming the polymer layer step is performed using a photo lithography process.

73. (previously presented) The method of claim 68 wherein the forming the conductive vias step comprises laser machining and thinning the base die.

74. (previously presented) The method of claim 68 further comprising following the bonding step, thinning the secondary die by grinding, polishing, or etching the secondary die.

75. (previously presented) A method for fabricating a semiconductor component comprising:

providing a base die comprising a substrate having a back side;

forming a plurality of conductive vias in the substrate;

providing a first secondary die comprising a circuit side, a plurality of contacts and a plurality of secondary conductive vias;

bonding the secondary die to the back side and the contacts to the conductive vias;

providing a second secondary die; and

bonding the second secondary die to the first secondary die in electrical communication with the secondary conductive vias.

76. (previously presented) The method of claim 75 further comprising forming a plurality of terminal contacts on the base die in electrical communication with the conductive vias.

77. (previously presented) The method of claim 75 further comprising thinning the first secondary die, the second secondary die and the base die.

78. (previously presented) The method of claim 75 wherein the forming the conductive vias step comprises laser machining openings in the substrate and then depositing a nano particle conductive polymer in the openings.

79. (previously presented) The method of claim 75 further comprising forming a polymer layer on the base die configured to protect and rigidify the component.

Claims 80-100 (canceled)

101. (currently amended) A method for fabricating a semiconductor component comprising:

providing a base die;

thinning the base die;

forming a conductive via in the base die;

forming a metal layer on the conductive via;

providing a secondary die comprising a contact; and

bonding the contact on the secondary die to the metal layer on the conductive via.

102. (previously presented) The method of claim 101 wherein the layer comprises a metal selected from the group consisting of nickel, zinc, chromium, palladium and gold.

103. (currently amended) The method of claim 101 further comprising thinning the secondary die following the bonding step.

~~wherein the layer comprises nickel.~~

104. (currently amended) The method of claim 101 wherein the forming the conductive via step comprises etching an opening in the base die and at least partially filling the opening with a conductive material.

~~further comprising thinning the base die prior to the bonding step.~~

105. (currently amended)) ~~The method of claim 101 wherein the secondary die comprises~~

A method for fabricating a semiconductor component comprising:

providing a base die;

forming a conductive via in the base die;

forming a metal layer on the conductive via;

providing a secondary die comprising a thinned die having a contact; and

bonding the contact on the secondary die to the metal layer on the conductive via.

106. (currently amended) The method of claim ~~101~~ 105 wherein the base die has a larger peripheral outline than the secondary die.

107. (currently amended) A method for fabricating a semiconductor component comprising:

providing a base die;

forming a plurality of conductive vias in the base die, each conductive via comprising a conductive material in an opening and a metal layer on the conductive material;

thinning the base die;

providing a secondary die comprising a plurality of contacts;

thinning the secondary die;

bonding the contacts on the secondary die to the conductive vias on the base die; and

forming a plurality of terminal contacts on the base die in electrical communication with the conductive vias.

108. (previously presented) The method of claim 107 wherein the conductive material comprises solder and the metal layer comprises nickel.

109. (currently amended) The method of claim 107 wherein the forming the conductive vias step comprises etching each opening.

~~further comprising thinning the base die and the secondary die prior to the bonding step.~~